

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/065,340
				Filing Date	10/06/2002
				First Named Inventor	MELVIN
				Art Unit	2186
				Examiner Name	S. Elmore
				Attorney Docket Number	
Sheet	1	of	3		

[illegible][illegible]

Examiner Signature	<i>S. Elmore</i>	Date Considered	9-1-2005
-----------------------	------------------	--------------------	----------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.**



INFORMATION DISCLOSURE STATEMENT BY APPLICANT - Page 3 of 3

Application Number: 10/065,340

Filing Date: 10/06/2002

Applicant: Stephen Waller Melvin

~~3-11-03~~ 3-11-03

Cite	Non Patent Publication
4	1 S. MELVIN and Y. PATT, "Handling of Packet Dependencies: A Critical Issue for Highly Parallel Network Processors," <i>International Conference on Compilers, Architecture, and Synthesis for Embedded Systems</i> , October 8-11, 2002, Grenoble, France
SE	2 M. FRANKLIN AND G. SOHI, "ARB: A hardware mechanism for dynamic reordering of memory references," <i>IEEE Transactions on Computers</i> , vol. 45, pp. 552-571, May 1996.
SE	3 S. GOPAL, T. N. VIJAKUMAR, J. E. SMITH AND G. S. SOHI, "Speculative versioning cache," <i>Proceedings of the Fourth International Symposium on High-Performance Computer Architecture</i> , Las Vegas, February 1998.
SE	4 G. SOHI, S. BREACH, AND T. VIJAYKUMAR, "Multiscalar processors," <i>Proceedings of the 22nd Annual International Symposium on Computer Architecture</i> , pp. 414-425, Ligure, Italy, June 1995.
SE	5 J. G. STEFFAN AND T. MOWRY, "The potential for using thread-level data speculation to facilitate automatic parallelization," <i>Proceedings of the Fourth International Symposium on High-Performance Computer Architecture</i> , Las Vegas, February, 1998.
SE	6 L. HAMMOND, M. WILLEY, AND KUNLE OLUKOTUN, "Data Speculation Support for a Chip Multiprocessor," <i>Proceedings of the Eighth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-VIII)</i> , San Jose, October 1998.
SE	7 J. STEFFAN, C. COLOHAN, ANTONIA ZHAI, AND T. MOWRY, "A Scalable Approach to Thread-Level Speculation," <i>Proceedings of the 27th Annual International Symposium on Computer Architecture</i> , Vancouver, Canada, June 2000.
SE	8 M. CINTRA, J. MARTINEZ, AND J. TORRELLAS, "Architectural Support for Scalable Speculative Parallelization in Shared-Memory Multiprocessors," <i>Proceedings of the 27th Annual International Symposium on Computer Architecture</i> , Vancouver, Canada, June 2000.
SE	9 J. MARTINEZ AND J. TORRELLAS, "Speculative Locks for Concurrent Execution of Critical Sections in Shared-Memory Multiprocessors," <i>Workshop on Memory Performance Issues, International Symposium on Computer Architecture</i> , Göteborg, Sweden, June, 2001.
SE	10 R. RAJWAR AND J. GOODMAN, "Speculative Lock Elision: Enabling Highly Concurrent Multithreaded Execution," <i>Proceedings of the 34th Annual International Symposium on Microarchitecture</i> , Austin, Texas, December 2001.
SE	11 M. HERLIHY AND J. E. B. MOSS, "Transactional Memory: Architectural support for lock-free data structures," <i>Proceedings of the International Conference on Computer Architecture</i> , pp. 289-300, San Diego, California, May 1993.

S. Elm

9-1-2005